DESIGN OF A DSP COMPUTER FOR RADIO-AMATEUR APPLICATIONS
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1. General Design

As already explained in the theoretical part of the article, I decided to design a computer with DSP capabilities around a standard 16 bit microprocessor, in particular the Motorola MC68010. An additional requirement was to design the hardware such that it does not slow down the CPU in any way due to the speed requirements of DSP algorithms.

The practical hardware design of a 16 bit microprocessor imposes many constraints. In comparison to a 8 bit microprocessor system, the number of connections is more than doubled. Further, 16 bit microprocessors have an order of magnitude faster bus than 8 bit microprocessors. Bus ringing and crosstalk, which are seldom a problem in a well designed 8 bit microcomputer, usually cause troubles in 16 bit designs. Professional computer designers generally solve the problem by using a better printed circuit board technology, namely multilayer printed circuit boards. The latter are prohibitively priced if a small quantity is only required and this technology is therefore out of reach for amateur experimental work.

For experimental work a modular design with a common bus board, carrying just several multi-pole connectors with all the pins connected in parallel, is necessary. After a careful analysis of the MC68010 bus signals I found out that a bus with 64 pole connectors could be sufficient. The selection fell on the well proven and reliable, but easily available and reasonably priced "Euro-card" connectors. A 64 pole "Euro-card" connector has two rows of 32 gold plated contacts. The required parallel connections can be made all on one side of a double-sided printed circuit board so that the other side can be used as an almost continuous ground plane to significantly reduce crosstalk between the signal lines.

Considering the technology I had available for the printed circuit boards: simple double sided boards with not too fine line geometry and not too many feed-through holes, the modules had to be made slightly larger than the standard "Euro-card" format. All the modules developed are 120mm wide and 170mm long. The modules represent functional units and all the connections among the modules themselves are made through the computer bus with "Euro-card" connectors.

Of course, the hardware design of a computer also depends on the application and software used. Since I decided right from the beginning to use nonvolatile RAM as the main program and data storage, the computer bus also carries a continuous supply voltage obtained from a single NiCd battery in the power supply module. The latter supplies all the computer memory and the real-time-clock circuit. Even more important, a nonvolatile RAM requires a very reliable RESET circuit. The latter should also be able to prevent the destruction of the data during any power-up or power-down sequence by inhibiting the access to the

RAM unless the supply voltage is within the specified
tolerances. The RESET signal is therefore generated by the
power supply module and made available to all computer modules
through the bus.

Since I planned little use of magnetic media, I made no
special arrangements for quick data transfer to or from the
computer memory. The computer has no DMA capability and the
MC68010 is hardwired to be the bus master all the time. In any
case, the MC68010 is fast enough to handle the data stream to
or from a floppy-disc controller on its own, without the aid of
a DMA controller. In the case of a DSP application with a
typical 10 kHz sampling frequency, not using a DMA controller
brings a penalty of only 10% or less in terms of CPU time.
Finally, for memory-to-memory transfers, the MC68010 Loop-Mode
instructions are almost as fast as a DMA controller.

In a 16 bit microcomputer design is frequently convenient
to use standard 8 bit peripheral devices because they are
in-expesive and widely available. Since these are usually too
slow to interface directly with a high speed 16 bit
microprocessor bus, additional interface circuits are required.
The latter are placed on the peripheral modules where required
due to the limited number of conductors available on the
computer bus.

2. MC68010 Operation

Before describing the various computer modules, a brief
description of the MC68010 CPU operation will be made. This
introduction is intended for the reader that has a basic
knowledge about the operation of a microcomputer, in particular
of a 8 bit microprocessor, but has little or no experience with
16 bit microprocessors.

The MC68010 has a 16 bit data bus and 32 bit internal
registers. All addresses are internally 32 bits long and are
referred to 8 bit bytes, corresponding to an addressing range
of 2^{32} or 4 tera-bytes. However, the upper 8 address bits are
not available externally (there are not enough pins on the
package), and the addressing range is limited to 2^{24} or 16
megabytes. There are only 23 address lines, A1 to A23, since
the 16 bit wide bus can access two bytes at a time. In the case
of a single byte access, only half of the available data lines
are used, either the lower 8 data lines D0 to D7 (odd address)
or the upper 8 data lines D8 to D15 (even address).

16 bit data words are always addressed by an even address
(LSB=0). A word access on an odd address (LSB=1) would require
two separate bus cycles. The MC680xx series of microprocessors
does not tolerate word accesses on odd addresses, in contrast
with some other 16 bit microprocessors, and a call to the
address error handling routine is generated. All MC68010
instruction codes are either one or an integer number of 16 bit
words and the program counter is always incremented in steps of
2, 4, 6 or other even numbers.

A typical memory access (read or write) cycle is shown on
Fig.1. The address lines A1 to A23 are set first, followed by

the Address Strobe (AS\) signal going low. Two data strobe
lines, Upper Data Strobe (UDS\) and Lower Data Strobe (LDS\)
select the byte to be accessed. In the case of a word access,
both UDS\ and LDS\ are asserted going low simultaneously. In
the case of a write cycle, the Read/Write (R/W\) signal goes
low before the data strobes. The microprocessor now waits for
the read or write operation to be completed. When the operation
is completed, the memory signals this to the microprocessor by
pulling the Data Transfer ACKnowledge (DTACK\) line low. If no
memory is available at the specified address, an external logic
is usually used to activate the Bus ERRor line (BERR\).
      The MC68010 supplies three additional signals, named
function codes FC0, FC1 and FC2, to better describe the type of
the bus cycle performed: instruction fetch, data read or write
in both user and supervisor modes or interrupt acknowledge.
Function code signals have to be decoded together with the
address lines A1 to A23 to select devices tied on the bus.
      The MC68010 accepts seven different interrupts with
differing priorities. The highest priority interrupt is not
maskable (NMI) while the other interrupt levels can be inhibited
by setting bits in the status register. The seven interrupt
requests are decoded from three input lines: IPL0\, IPL1\ and
IPL2\, to reduce the number of pins on the microprocessor
package. An external priority encoder (usually 74LS148) is
required in most applications.
      CLOCK is obviously required by the microprocessor itself.
RESET\ and HALT\ are both inputs: to reset the microprocessor,
and outputs: to reset the peripherals under program control and
signal a double bus error. Additional control lines include an
interface for the slow 6800 series peripherals (VPA\, E, VMA\)
and bus request lines for DMA (BR\, BG\, BGACK\).
      Most of the microprocessor signals are brought to the
computer bus without using buffers. The latter are placed on
the inputs of the various modules to reduce bus loading. The
actual bus connections on a 64 pole "Euro-card" connector are
shown on Fig.2.

3. Processor Board

      The processor board includes the MC68010 chip and
corresponding support circuitry, up to 32 kbytes of EPROM
containing the operating system, 64 kbytes of nonvolatile RAM
and the real-time calender/clock. The corresponding circuit
diagram is shown on Fig.3 and Fig.4.
      The microprocessor support circuits include a clock
generator, a bus-error timer, an interrupt-request priority
encoder, an interrupt auto-vector logic, a reset logic and and
address decoder for the remaining on-board devices. The clock
generator is a simple crystal oscillator built around a CMOS
(HC) gate, since there are no special requirements regarding
its accuracy. The nominal clock frequency is 10 MHz. Additional
HC gates are used to buffer the oscillator output.
      The bus-error timer monitors the AS\ signal. In the case
of a bus-error no device will answer with a DTACK\ or VPA\ to

terminate the bus cycle and the AS\ could remain low indefinitely. However, the AS\ is also used to reset the bus-error timer. If the AS\ remains low for more than 192 clock cycles, the bus-error timeout counter (LS393) will assert the BERR\ signal commanding the MC68010 to call the bus-error handling routine.

The interrupt-request priority encoder is simply a LS148 with pull-up resistors on its active-low inputs, so that more devices requesting the same level interrupt can be simply wired-or. The MC68010 is used in the auto-vector mode. The latter is invoked by decoding the interrupt-acknowledge function code (all three FC outputs at logical high) and asserting the VPA\ signal.

The MC68010 microprocessor is reset when both RESET\ and HALT\ lines are pulled low simultaneously for a sufficiently long period of time: at least 10 clock cycles during normal operation but at least 100 milliseconds after power-up. The reason for this long power-up reset time is easily explained since the MC68010 is a dynamic NMOS circuit internally. The delay of 100 ms is required for the internal on-chip substrate bias-generator to achieve its full output voltage of about -3V. The Main Reset signal (MR\), supplied from the power-supply module, is applied through open-collector gates to both RESET\ and HALT\.

The MC68010 RESET\ pin can also be an open-drain output, activated when executing the RESET instruction. The latter will not reset the microprocessor but will drive the RESET\ pin low for 124 clock cycles. This signal is made available on the computer bus and is used to reset all peripheral devices.

On the other hand, the HALT\ pin is driven low when a double bus-error is detected after a software crash or hardware failure. A double bus-error blocks the MC68010 to avoid damaging the memory content allowing subsequent troubleshooting. After a double bus-error a reset is required to restart the MC68010.

The address decoder is used to select the on-board memories and peripherals decoding the most significant address lines and to answer with a DTACK\ or a VPA\ signal. The nonvolatile CMOS RAM requires an additional decoder chip (HC138) which receives the same battery-backed supply voltage as the RAM itself. The decoder is inhibited by the MR\ signal to protect the RAM content during power-up or power-down.

A single 8 bit wide EPROM is used to store the operating system software. A 8 bit latch (LS374) and a sequence generator (LS164) are used to generate a 16 bit data word for the MC68010. Since the this sequential 8+8 bit read operation is slow, the software is copied into the on-board system RAM immediately after reset. Once in the RAM, the software can be executed at full speed with no processor wait states.

The lower 16 kbytes of the on-board system RAM are assigned to the stack by the present software. In the case of a software crash it is usual for the stack to grow in an uncontrolled way. Therefore the locations immediately below the stack area are not assigned to any device so that an uncontrolled stack growth ends in a double bus-error safely blocking the MC68010.

A 71055 parallel I/O port (fast CMOS version of the popular 8255) is used to interface the keyboard and the real-time clock chip. The parallel keyboard output is connected to port A, configured as a strobed input. Port B is a spare output. The remaining bits of port C are used both as inputs and as outputs to interface the 4990 real-time clock chip. The latter has serial inputs and outputs. Clocks and other signals are generated by software.

The 4990 Chip Select (CS) input is driven by the MR\ signal to protect the clock count during power-up or power-down for the same reason as the nonvolatile RAM. The 4990 has an on-chip open-drain interrupt output while the keyboard interrupt, generated inside the 71055, requires an additional transistor. Current software requires the clock interrupt on INT1\ and the keyboard interrupt on INT7\, selectable through jumpers on the printed circuit board.

4. Video Board

The video board includes 128 kbytes of special, dual-port video RAM, video D/A converter and timing and interface circuits. The circuit diagram of the video board is shown on Fig.5 and Fig.6.

The memory used in a video interface is being read continuously to update the picture displayed on a CRT several times per second. If a microprocessor has to access the same memory, for example to update the picture, it can either wait for the horizontal or vertical retrace period or interrupt the display read operation disturbing the picture. General purpose dynamic or static memories are usually not fast enough to provide data for a high resolution video signal generation and be accessed by a fast 16 bit microprocessor at the same time. On the other hand, true dual-port memories with two completely independent access ports are both difficult to manufacture and expensive.

A few years ago semiconductor manufacturers invented an alternative solution to increase the data rate from a dynamic memory built using only conventional DRAM chip technology. During any random access read or write operation, inside a dynamic RAM a whole row of data (1024 bits in a 256 kbit RAM) is transferred from its storage cells to as many refresh amplifiers. This data can not be transferred quickly only because it is completely impractical to build an IC housing with so many pins. However, this data can be transferred to another circuit efficiently if the latter is located on the same semiconductor chip.

Dual-port dynamic memories include on-chip an additional shift register. A whole row of bits can be transferred from the main memory array to the auxiliary shift register in one single operation, called a data-transfer cycle and lasting no more than an ordinary data-access cycle. After such a data-transfer cycle the dynamic memory circuits and the shift register are completely independent: the microprocessor can randomly access the data in the main memory array (with no

timing penalties) while other data is shifted out of the
auxiliary register to generate the video signal.

Since dual-port video memories are only slightly more
expensive than conventional dynamic RAMs, they are very
attractive for any new video memory design. A data-transfer
cycle usually has to be performed once every television line:
once every 64 microseconds and it takes less than 1% of this
time. The memory is therefore available to the microprocessor
for more than 99% of the total time with no delays or disturbs
to the generated video.

The described video board uses four 41264 chips which are
organized as 64k by 4 bits each. From the microprocessor side
the video memory is organized as 64k 16 bit words, from the
video side there are 128k pixels arranged in 256 lines of 512
pixels each and the intensity of each pixel is described with
8 bits or 256 possible grey levels. Each 41264 chip also has
four 256 bit shift registers that are all loaded in a single
data-transfer cycle occurring during the horizontal retrace
period. During the active scanning period, data is retrieved
alternatively from two shift register groups so that the
position of the 512 pixels obtained matches the microprocessor
byte address ennumeration simplifying and speeding-up the
the software.

All the timing of the generated video signal is derived
from an on-board 12 MHz crystal oscillator, which drives a
divider chain. The line period matches the standard TV line
period (64 us). One TV line consists of 768 pixels: two thirds
(512 pixels) represent the useful scan and the remaining third
(256 pixels) is left for the horizontal retrace and black edges
at both picture sides. The number of lines in a TV frame is
slightly larger than standard: a frame of 320 lines was
selected for simplicity. To avoid flicker the scanning is not
interlaced.

At the end of each useful scan period the video timing
logic issues a request for a data-transfer cycle to obtain the
data for the next television line. The request can not be
granted immediately since the microprocessor may be using the
memory at the same time. All dynamic memories are very
sensitive to correct timing: any incorrect timing access cycle
disturbs the refresh operation and destroys immediately at least
one whole row of data!

The data-transfer cycle request is therefore passed to an
arbitration logic, built around a double JK-FF (LS112). The
arbitration circuit decides who has priority to access the
memory, allowing the device currently accessing the memory to
complete the cycle in a regular way. In the worst case, the
microprocessor has to wait for one complete data-transfer cycle
or the video timing logic has to wait for one microprocessor
bus cycle.

The data-transfer cycle timing is generated by a
sequential logic with a 8 bit shift-register (LS164) and
corresponding gates. Like all dynamic memories, the 41264
require RAS\ and CAS\ clocks and address multiplexing. LS244
tri-state buffers are used for both row and column address
multiplexing and for switching the address lines between the
microprocessor and the video timing logic. Since the

microprocessor may want to access a single byte at a time, separate CAS\ clocks are derived from UDS\ and LDS\.

The 41264 video RAM serial outputs have tri-state capability and are simply tied in parallel for multiplexing. A fast 8 bit D-FF (S374) is however required to "clean" the data in front of the video D/A converter. During both horizontal and vertical retrace periods all the 8 data lines are held low (black level) by a tri-state buffer (LS244).

Sync pulses are added to the output of the D/A converter. The horizontal sync pulse is generated by a dual monostable and its position can be adjusted to match the monitor used. The vertical sync pulse is generated by a dual FF, it is two line periods long and occurs 32 lines after the end of the useful picture scan.

A 733 video amp is used to boost the generated video signal level. Both polarities are available to drive any type of standard-scan TV monitor. Both the D/A converter and the video amplifier require a negative supply voltage of about -4V that is generated on-board. All supply voltages of the analog part of the circuit are to be well filtered to avoid disturbs in the video signal.

5. Memory

For most application programs, especially those handling pictures, the computer requires much more memory than the 64 kbytes provided on the processor board. Out of the MC68010 16 Mbyte addressing range the current operating system uses the first megabyte for various system functions: start-up ROM, stack, video memory and I/O port addresses. The remaining 15 Mbytes are intended for memory expansion.

The circuit diagram of a 256 kbyte nonvolatile memory board is shown on Fig.7. The circuit includes eight 256 kbit CMOS RAMs 43256, address and data buffers to decrease the capacitive loading of the computer bus and an address decoder. The start address of the 256 kbyte block can be selected to start anywhere from address 200000H to 3C0000H positioning an on-board jumper.

The 43256 memory chips only have an active-low chip-enable input. To preserve the memory content when the computer is switched off, the chip-enables have to be kept high. This requirement can be met easily using a CMOS (HC) address decoder (HC138) supplied from the same rail as the memory chips. The address decoder has an active-high input tied to MR\ to protect the memory content.

In a typical system, 4 such memory boards are used for a total 1 Mbyte nonvolatile memory. The latter is enough for most DSP applications and for some simple image processing. Due to bus loading problems it is difficult to connect more than 4 memory boards without sacrifying the operating speed. Of course as soon as higher density memory chips become available, the described memory boards will be replaced by a higher capacity memory.

6. Analog I/O

  An important part of any DSP computer is its interface to the analog world. As already described in the theoretical part, I decided to use a telephone CODEC IC as the A/D and D/A converter, since its performances match those of voice grade communications receivers and transmitters, including radio-amateur receivers and transmitters. Since all CODECs have on-chip a serial data interface, a UART is required to interface a CODEC to a microprocessor. Programmable counters are used to generate the A/D and D/A sampling rates.

  The analog I/O board also includes an independent RS-232 interface. The circuit diagram is shown on Fig.8 and Fig.9. The RS-232 UART (71051), the programmable counters (71054) and the UART to interface the CODEC (another 71051) are all standard 8 bit microprocessor peripherals. To interface the faster MC68010 bus, a timing logic built around a 4 bit shift register (LS195) is required. The logic is started whenever any of the three on-board peripheral chips are selected by the address decoder (two LS138), generating a longer Read (R\) or Write (W\) pulse and finally terminating the bus cycle by issuing a DTACK\ to the MC68010. All three peripherals are connected to the lower byte (D0 to D7) of the 16 bit data bus through a bidirectional buffer (LS245) to reduce the capacitive bus loading.

  The RS-232 UART is equipped with a standard RS-232 receiver (75154). A 4053 CMOS multiplexer is used to generate RS-232 compatible transmit signal levels out of the +5V and -5V supplies available on-board. The RS-232 UART generates both receive (RX buffer full) and transmit (TX buffer empty) interrupts, connected through jumpers to INT3\ and INT2\ respectively. Both RX and TX clocks of the RS-232 UART are connected to a common programmable counter. The TX baud-rate therefore can not be programmed different from the RX baud-rate.

  The CODEC UART has two separate programmable counters to generate the A/D and D/A sampling rates independently. Some additional logic, two 4029 counters and a few gates, are required to interface the MK5156 CODEC. The A/D generated interrupt (new data available) is connected to INT6\ and the D/A interrupt (new data required) is connected to INT5\.

  All the timing is derived from an on-board crystal oscillator at 6144 kHz. Some DSP programs, like the weather satellite picture receiving program, require a very accurate sampling frequency. The 6144 kHz clock is used by the UARTs, divided by 3 to obtain 2048 kHz required by the CODEC and switched-capacitor filter, divided by 2 to obtain 3072 kHz for the timing logic and divided by 4 to obtain 1536 kHz as the input to the programmable dividers. The divider by 3 is a little more complex to obtain a nearly 50% duty cycle at 2048 kHz.

  To interface directly with analog circuits: receivers or transmitters, the CODEC analog input and output are connected connected to a switched-capacitor filter (TP3040). The input

audio signal is applied to a bandpass filter with a lower
cutoff frequency of 300 Hz and an upper cutoff frequency of
3400 Hz before reaching the A/D converter. The D/A output
signal is applied to a low-pass with a cutoff frequency of
3400 Hz.

Additional command lines are also provided: one input and
two outputs. Their function is software programmable. The input
is usually used as a squelch input (high means valid analog
signal). The outputs are used as PTT and CW KEY commands to
a transmitter. These two outputs are open-collector and
active-low as required by most transmitters. The 75452 driver
can handle 300 mA and 30V on each of these outputs.

The CODEC, the switched-capacitor filter and the RS-232
driver require a negative voltage of -5V. The latter is
obtained on-board with a simple two-transistor flyback inverter
similar to that on the video board. The supply voltages of the
analog circuits have to be further filtered to avoid any
interference from the noisy computer bus +5V supply rail or
inverter. The CODEC also requires two reference voltages. The
positive reference is obtained from a red LED providing a
stable voltage drop of about 1.8V. The negative reference
tracks the positive reference to avoid distortion using an
op-amp (741).

7. Floppy Disk Drive

Although the operating system developed for my DSP
computer does not require a mass memory like magnetic disks for
its operation, it is very comfortable to have available a
floppy drive. For example, applications programs can be loaded
conveniently from a floppy disk for the first time, when
initializing the system. Floppy disks are also useful for
backup copies and to store large amounts of data for longer
periods of time (pictures).

Building the mechanical part of a high performance floppy
drive is probably out-of-reach for an amateur. Available floppy
drives come already with some electronics like write and read
head amplifiers and motor drivers. Most of the recent floppy
drives come with a 34 pole connector carrying TTL level signals
in both directions. These signals are standardized. There are
also many special purpose chips available, called Floppy Disc
Controllers (FDC), to interface the standard "34 pole
connector" signals to any microprocessor or DMA controller.

I selected to use 3.5" double-sided floppy discs on a
300 rpm drive at a recording speed of 250 kbps MFM. A 80 track
double-sided disk has a raw capacity of 1 Mbyte. Each track has
a raw capacity of 6.25 kbytes and the current software formats
it into 5 sectors of 1024 bytes each, resulting in a formatted
capacity of 800 kbytes per disk.

Floppy disk controllers come either in one chip or as a
set of chips. The Western Digital 2797 is a single-chip FDC
with an analog data separation PLL. New FDCs have digital
PLLs that do not require adjustments, but the 2797 is cheap and
easily available. To interface a standard 3.5" floppy drive it

only requires a few open-collector, high-current-sink TTL buffers.

The circuit shown on Fig.10 and Fig.11 also includes some additional logic to make all of the 2797 functions selectable by software. The circuit to interface the slow 2797 to the fast MC68010 bus is identical to that used on the analog I/O board. A simple high-speed serial interface, based on a 8530 Serial Communications Controller (SCC), is located on the same board.

The timing for the FDC and bus interface logic is derived from a 16 MHz crystal oscillator. Its frequency is divided down to either 1 or 2 MHz to drive the 2797 clock input in the write mode. In the read mode, the 2797 derives its clocks from an on-chip PLL with a VCO running at 4 MHz.

To maintain software compatibility with its predecessors, the designers of the 2797 chip could not implement all of its functions as control register bits. The corresponding selection pins have to be driven by an additional output port, in this case a LS273 latch. Two outputs of the LS273 are used to select the floppy drive directly, bypassing the 2797 chip.

3.5" floppy drives do not have a head load solenoid: the read/write heads are loaded immediately after the disk is inserted into the drive. To avoid unnecessary wear of the disk and heads, it is necessary to stop the spindle motor after read or write operations are completed. In the case of the 2797 FDC, its Head LoaD (HLD) signal has to be used as a Motor On (MO) signal for a 3.5" floppy drive. Correspondingly, the READY input of the 2797 can not be used and the READY output from the drive, if available, should be tied to the Head Load Timing input of the 2797. The HLD output of the 2797 has an interesting feature: if not disabled by software it will be disabled automatically after 15 disk revolutions (3 seconds) following the last read or write operation. A software crash or a careless programmer will not destroy the disk nor damage the heads!

Some of the connections between the FDC and the 34 pole connector are brought to a jumper plug to adapt for small differences in the connections of different drives. The two 2797 interrupts, DRQ and INTRQ, are also connected through jumpers to INT4\ and INT3\ respectively.

The serial communications controller chip (8530) obtains all its timing from a 6144 kHz crystal oscillator, since this frequency can be divided to obtain standard baud rates. The serial port uses the same signal levels as the floppy drive interface: drivers are open-collector, high-current-sink TTL drivers and receivers are simple TTL inputs with pull-up resistors. INT6\ is assigned to the SCC, again through a jumper, to handle the high data rates expected.

8. Power Supply

Although the design of a power supply is not considered very important by most design engineers, power supplies are usually a major source of troubles in practical electronic circuits, especially computers! Overheating, electrical

interferences and unreliable resetting are common problems associated with poorly designed computer power supplies.

A DSP computer is intended to operate together with other analog equipment including sensitive receivers and powerful transmitters. Efficient shielding is a must to avoid interferences in both directions. However, an efficient shielding enclosure is normally very poor from the thermal design point of view since computer chips dissipate most of the heat produced by convection cooling. While it may not be possible to influence the amount of heat produced in the computer chips, other heat sources can be avoided in a careful design. A good efficiency, switching power supply is a must!

The circuit diagram of the recommended power supply for the DSP computer is shown on Fig.12. The power supply is intended to operate from a non-regulated DC supply of nominally 12V DC, negative grounded, like most other radio-amateur equipment. The efficiency of the simple series switching regulator is above 80%. Chokes at both input and output are used to suppress both interferences generated by the computer and by the switching regulator itself.

The power supply module includes a 3.6V, 500 mAh NiCd battery for clock and memory backup.

The reset circuit is an integral part of the power supply, since it is very difficult to derive the information to operate a reset circuit just from the +5V rail on the computer bus. The RESET\ signal will be applied immediately after the input voltage falls below about 6.5V. The series regulator is still operating correctly at this input voltage and the RESET\ signal will effectively protect the vulnerable content of the nonvolatile RAM. If the input voltage falls down to zero, the RESET\ signal remains active, since it is active-low.

When the input voltage is applied again, the RESET\ will only be removed after the input voltage goes above about 7V (hysteresis of about 0.5V) and after the delay introduced by the 1000uF/1.2kohm time constant. Everyday practical use confirmed that this resetting/protection scheme is failure-proof regardless of the kind of transients on the power line, in severe contrast to what happens with commercial computers, packet-radio TNCs or other equipment using microprocessors!

Since there are just four wires connecting the power supply module to the computer bus: +5V, +CMOS, MR\ and GND, the module is not equipped with an "Euro-card" connector to avoid capacitive loading of the computer bus.

9. Antenna Rotator Interface

Automatic satellite tracking with a steerable antenna system is usually required together with many DSP applications. The described DSP computer is able to generate the required tracking information as a background task to the main DSP task with a minimum additional loading of the CPU. Even in the case of updating the antenna pointing direction every second only about 2% of the total CPU time is required for the tracking

program.

Due to the variety of different antenna rotator systems I decided not to build any rotator interface inside the computer itself. The rotator interface shown on Fig.13 accepts data from the computer RS-232 port and interfaces to a KR-5600 rotator control unit. It includes a 8 bit microprocessor 5080 (CMOS version of the Z80CPU) with an EPROM (27C64) and a RAM (6116), an A/D converter (ADC0804), Darlington relay drivers (2004) and a simplified RS-232 port. Only a very small part of both the EPROM and the RAM are actually used since the software is very simple.

The rotator interface receives the desired antenna azimuth and elevation from the DSP computer. These values are compared with the actual values measured by the position-sensing potentiometers installed on the rotators and the interface microcomputer decides to activate the motors in the appropriate direction. The software also corrects for the inertia of the rotator and antenna system. The damping coefficients are also uploaded from the DSP computer. The interface also transmits a complete status report on request from the main computer.

All of the microcomputer components are CMOS versions to keep the current drain low. The overall current consumption of the interface is only about 35 mA. The latter can be derived from the multi-pole connector on the KR-5600 control unit thus saving the expense of an additional power supply. The interface requires just +5V obtained from a three-terminal voltage regulator. The A/D converter has its own 2.5V reference LM336. Since the computer memory content is lost after power-down, no special reset circuit is required, an RC network and a Schmitt-trigger gate are sufficient.

The RS-232 serial/parallel and parallel/serial conversions are done in software. Therefore, all the clocks are derived from a single crystal oscillator at 10 MHz: divided by 4 to obtain 2.5 MHz for the CPU and divided by 16 to obtain 625 kHz for the A/D converter.

A parallel I/O port (71055) controls the relay drivers, the analog multiplexer (4066) for the A/D converter and the RS-232 signals. The latter are not completely to the RS-232 specifications, since the output logical low is only zero volts, but are accepted by most RS-232 receivers. With suitable software the interface could be used with any computer equipped with a RS-232 port.

10. Future Plans

A construction article is planned to follow, discussing also hardware checkout, software installation and use of the DSP computer. Some information, like the operating system manual, can not be published since they would take far too much space in the magazine: copies will be made available separately. Software will probably be made available on floppy disks, including source files, their corresponding compiled versions and "manual" files describing how to use them.

There will certainly be many upgrades of both the hardware

and especially the software. A very successful upgrade was the replacement of all LS-series TTL integrated circuits with the new HC-series. The HC-series integrated circuits, now available at the same price as the older LSs, offer a much lower current consumption (power dissipation!) and a lower bus loading. In addition, their constant, resistive output impedance efficiently suppresses bus ringing, allowing up to 30% higher CPU clock frequencies.

The next imminent hardware upgrade is certainly a higher capacity memory board. Other peripherals could be built as well, including "intelligent" ones carrying maybe an even more powerful processor than the MC68010 or a dedicated DSP chip. On the other hand, future antenna rotators will probably include a RS-232 interface and the described rotator interface board will probably become unnecessary.

Of course, most upgrades can be expected in the software. Several algorithms, including the Fast Fourier Transform, have not even been tried yet, although it is known they are possible on the described hardware.
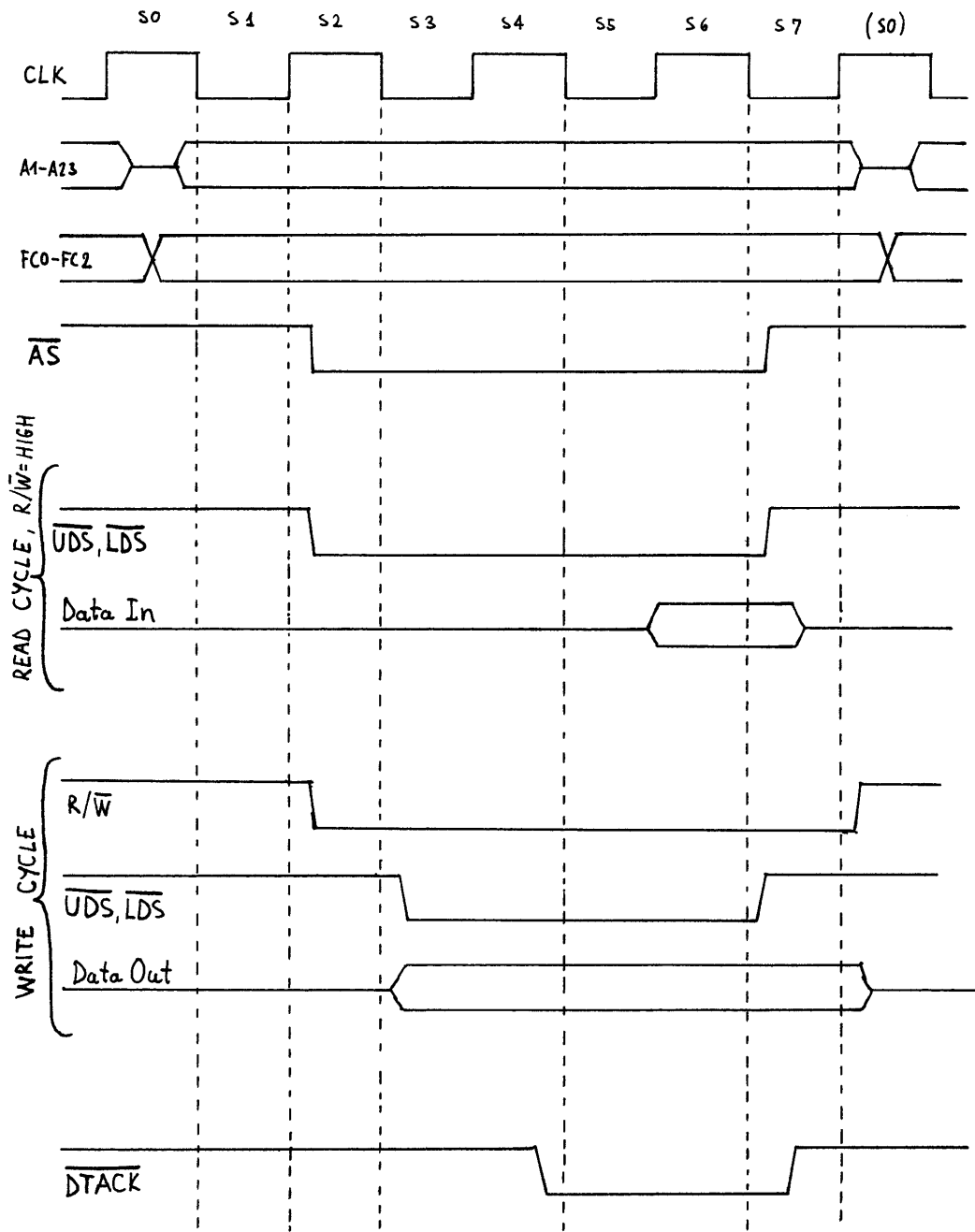

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Fig. 1 – MC68010 bus cycle timing.

C		A
GND	1	GND
D4	2	D5
D3	3	D6
D2	4	D7
D1	5	D8
DØ	6	D9
$\overline{AS}$	7	D10
$\overline{UDS}$	8	D11
$\overline{LDS}$	9	D12
R/$\overline{W}$	10	D13
$\overline{DTACK}$	11	D14
D15	12	A23
A22	13	A21
CLK	14	A20
$\overline{HALT}$	15	A19
$\overline{RESET}$	16	A18
A17	17	A16
$\overline{VPA}$	18	A15
FC2	19	A14
FC1	20	A13
FCØ	21	A12
A1	22	A11
A2	23	A10
A3	24	A9
A8	25	A7
A6	26	A5
A4	27	$\overline{INT7}$
$\overline{INT6}$	28	$\overline{INT5}$
$\overline{INT4}$	29	$\overline{INT1}$
$\overline{MR}$	30	$\overline{INT2}$
+CMOS	31	$\overline{INT3}$
+5V	32	+5V

Fig. 2 — Bus connections
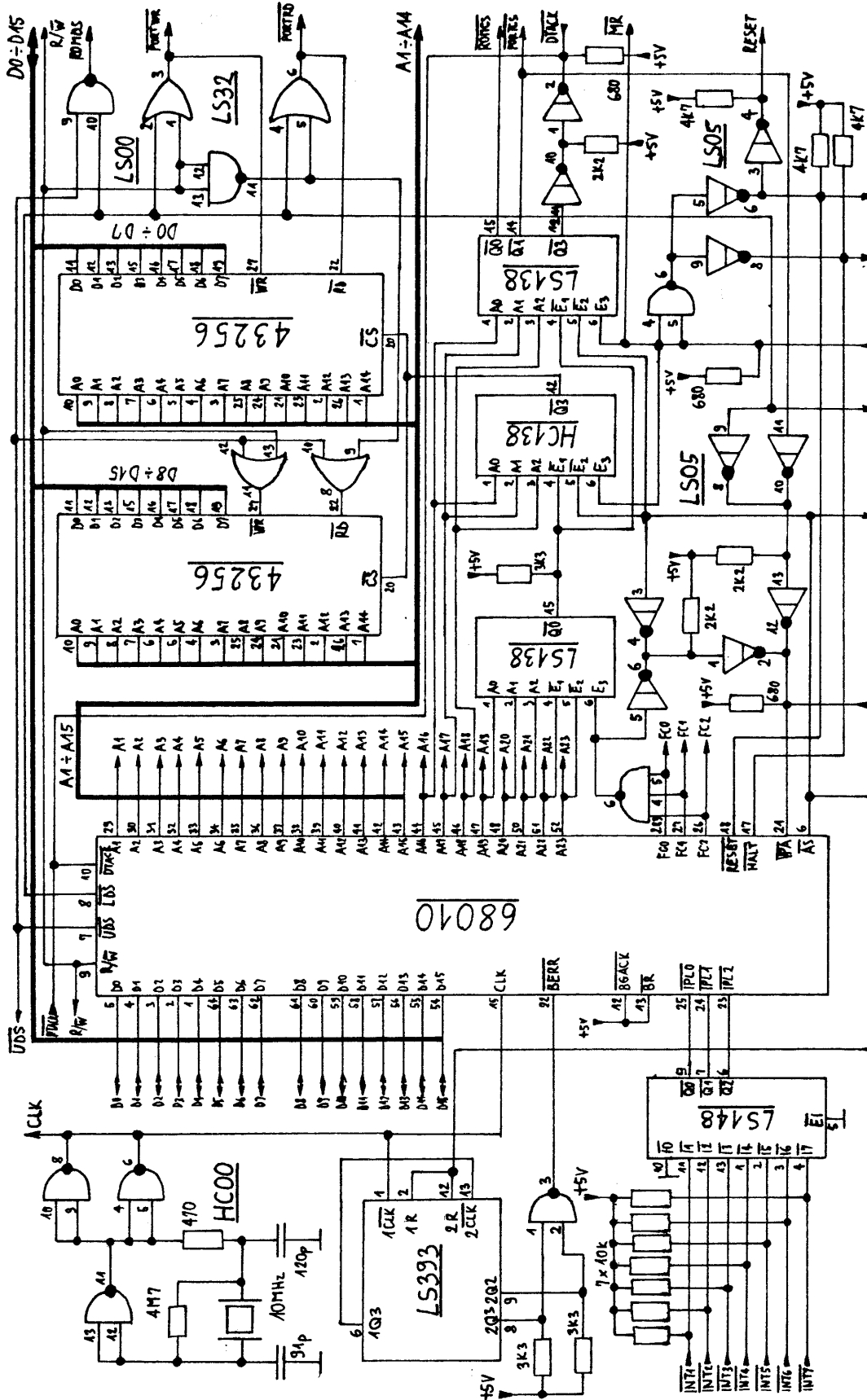
Fig. 3 — CPU board circuit diagram (part 1).
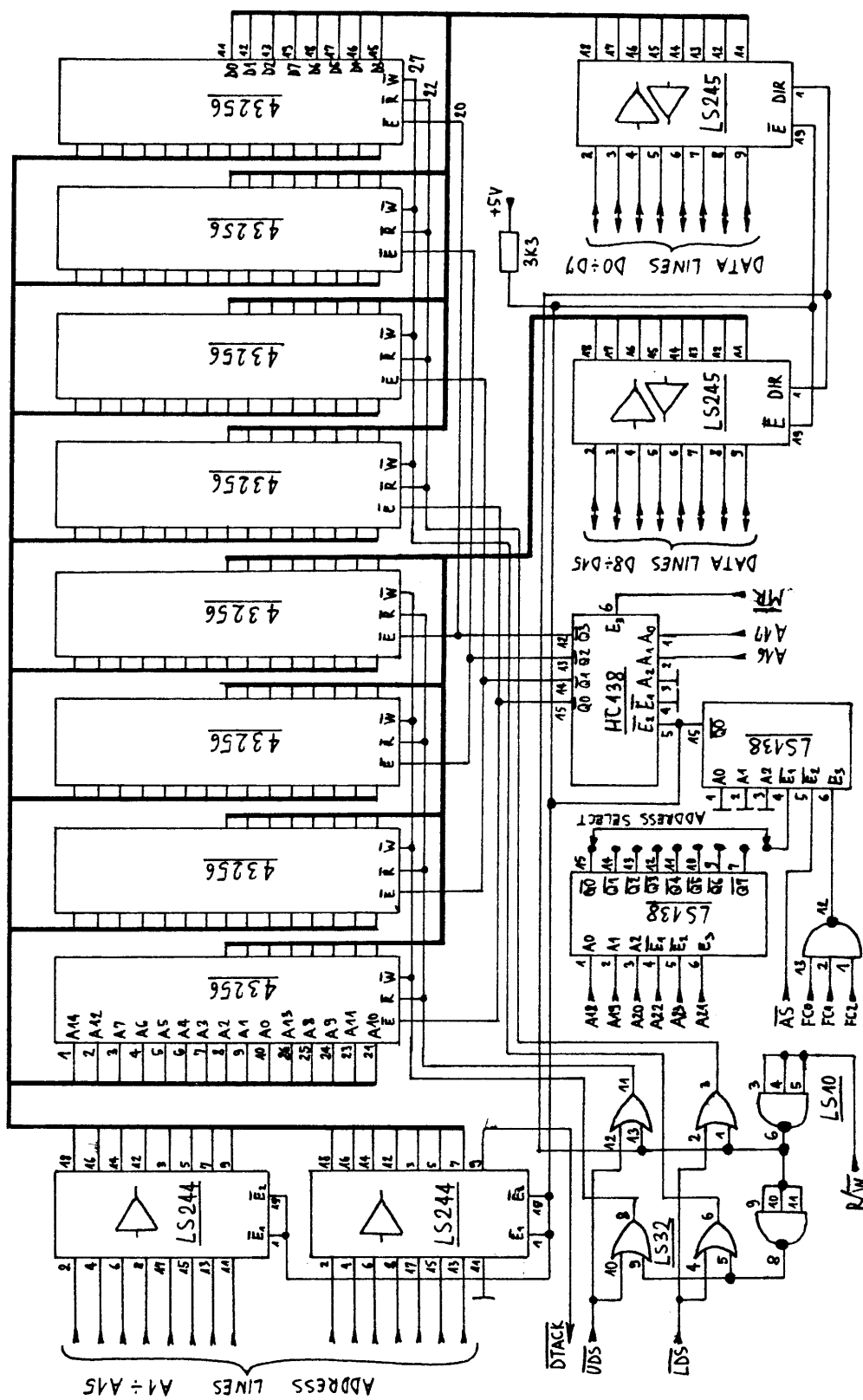
Fig. 4 — CPU board circuit diagram (part 2).

Fig. 5 - Video board circuit diagram (part 1).
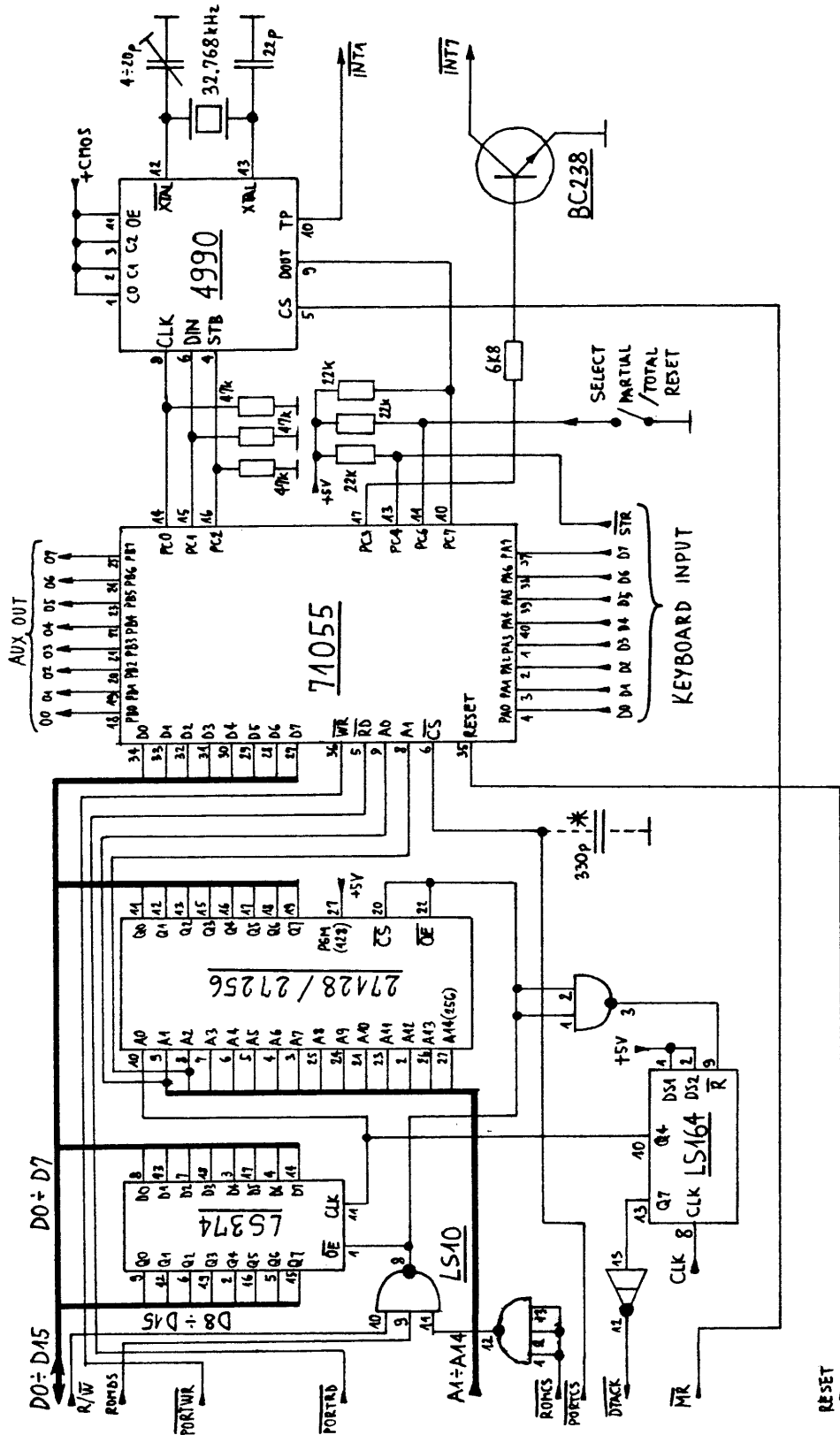
Fig. 6 - Video board circuit diagram (part 2).

Fig. 7 — 256k CMOS memory board circuit diagram.

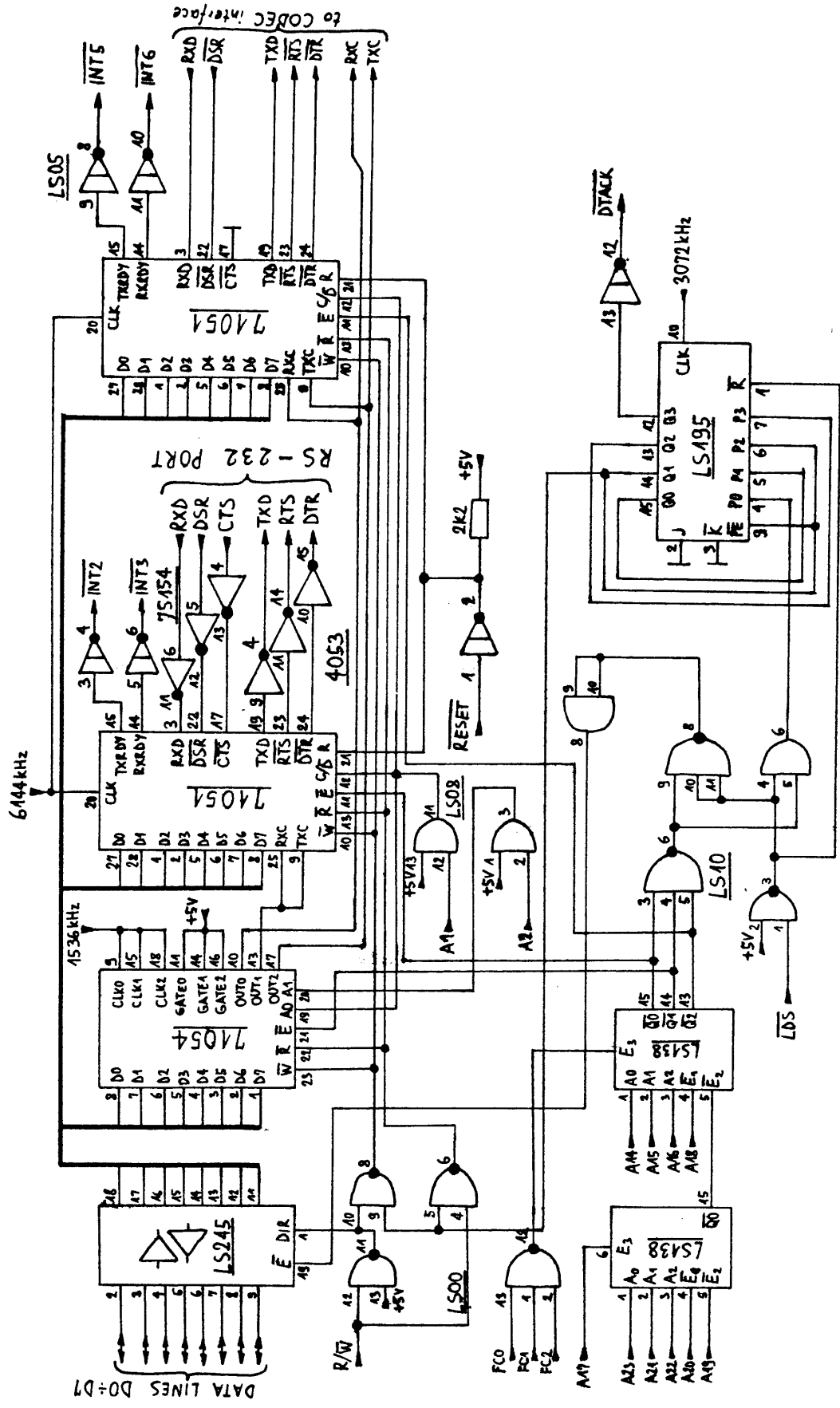Fig. 8 — Analog I/O and RS-232 board circuit diagram (part 1).

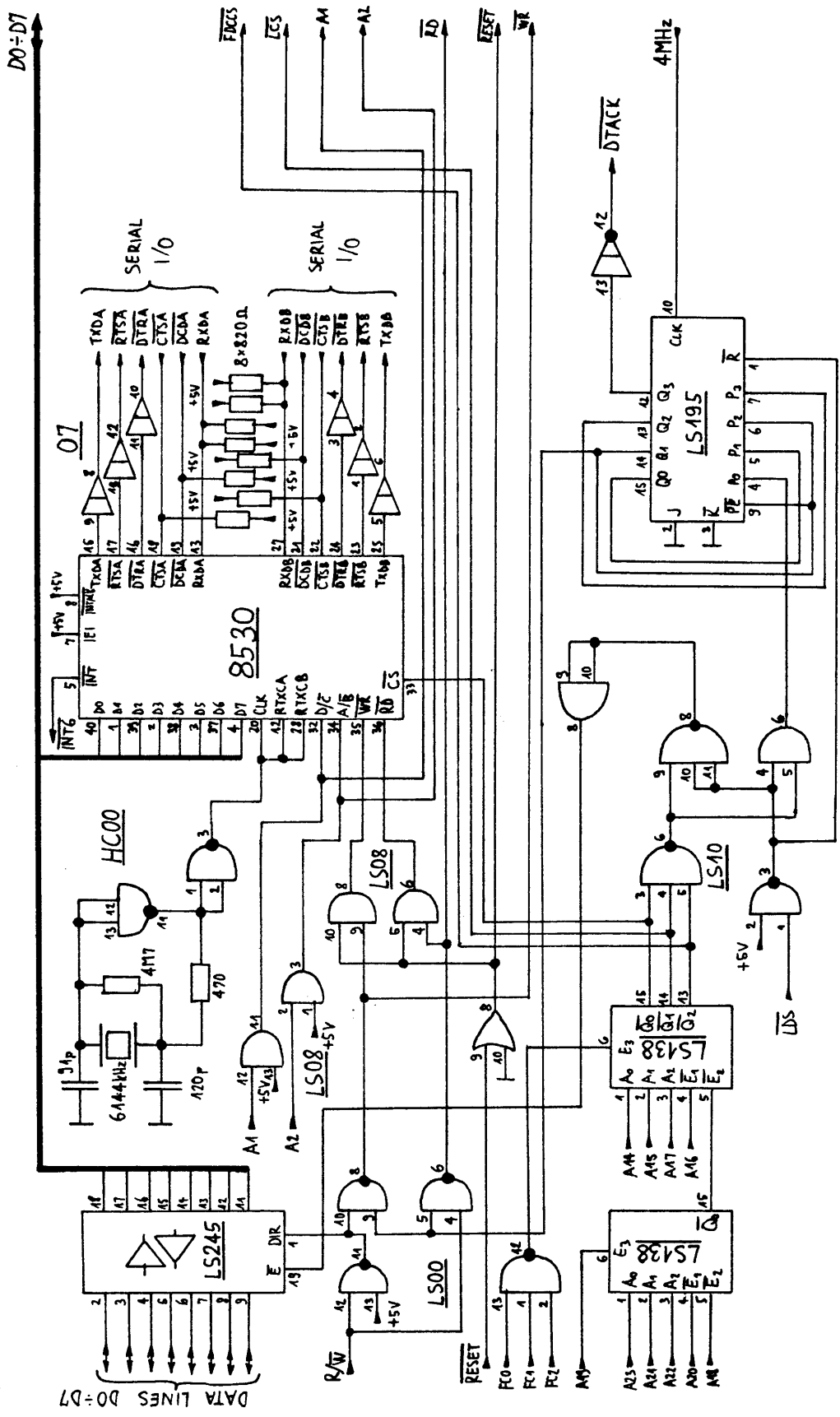Fig. 9 - Analog I/O and RS-232 board circuit diagram (part 2).

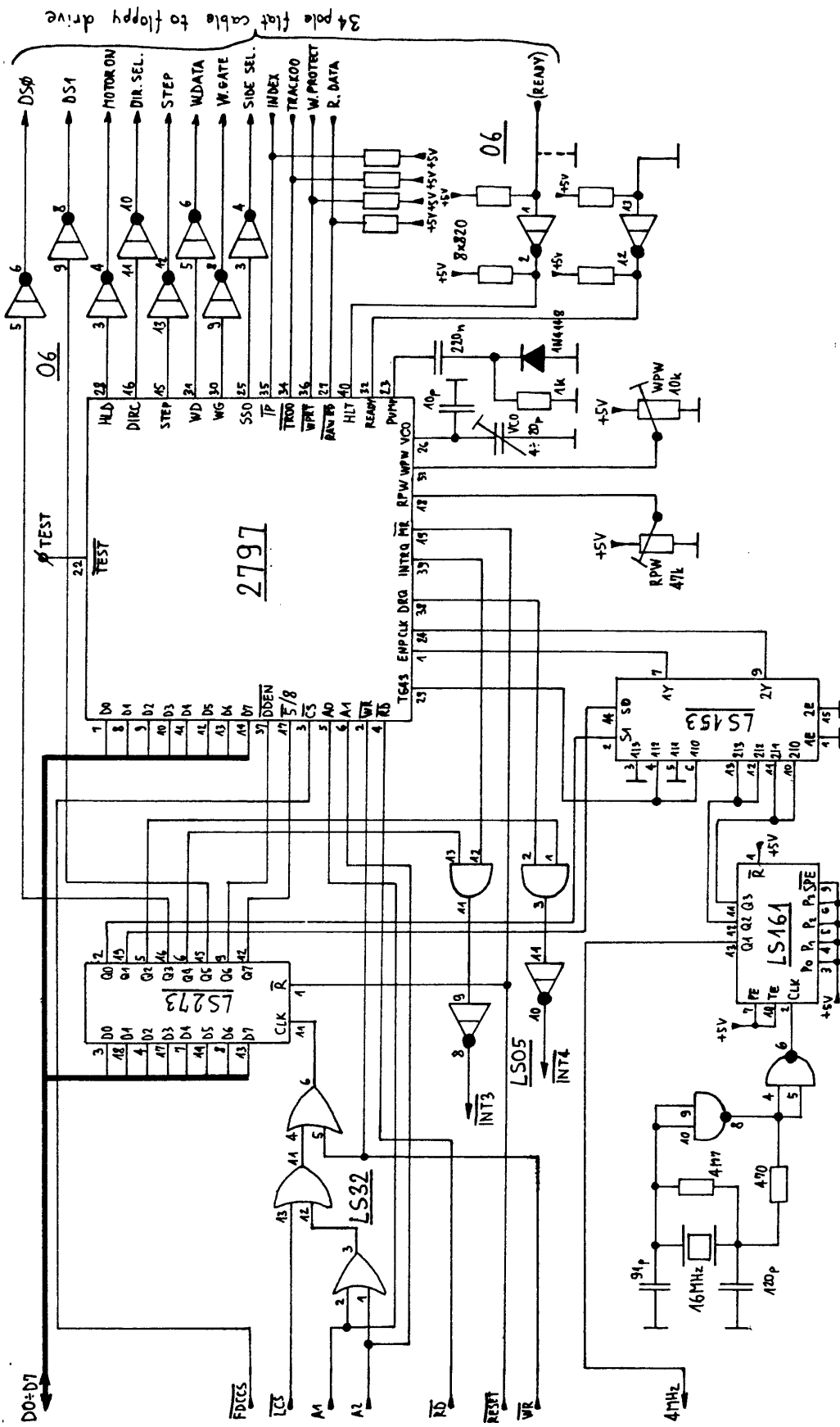Fig. 10 - Serial I/O and floppy interface board circuit diagram (part 1).

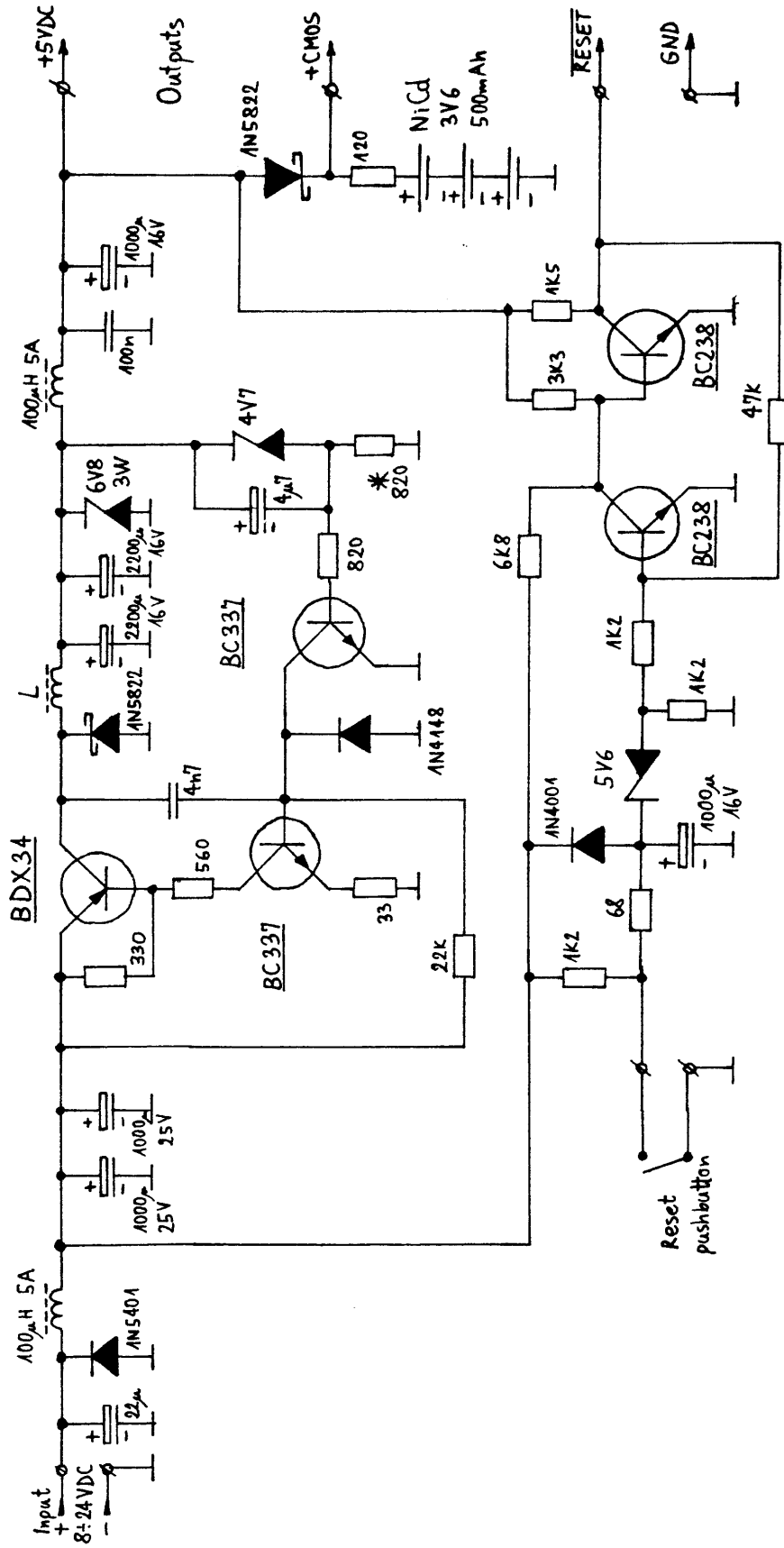Fig. 11 - Serial I/O and floppy interface board circuit diagram (part 2).
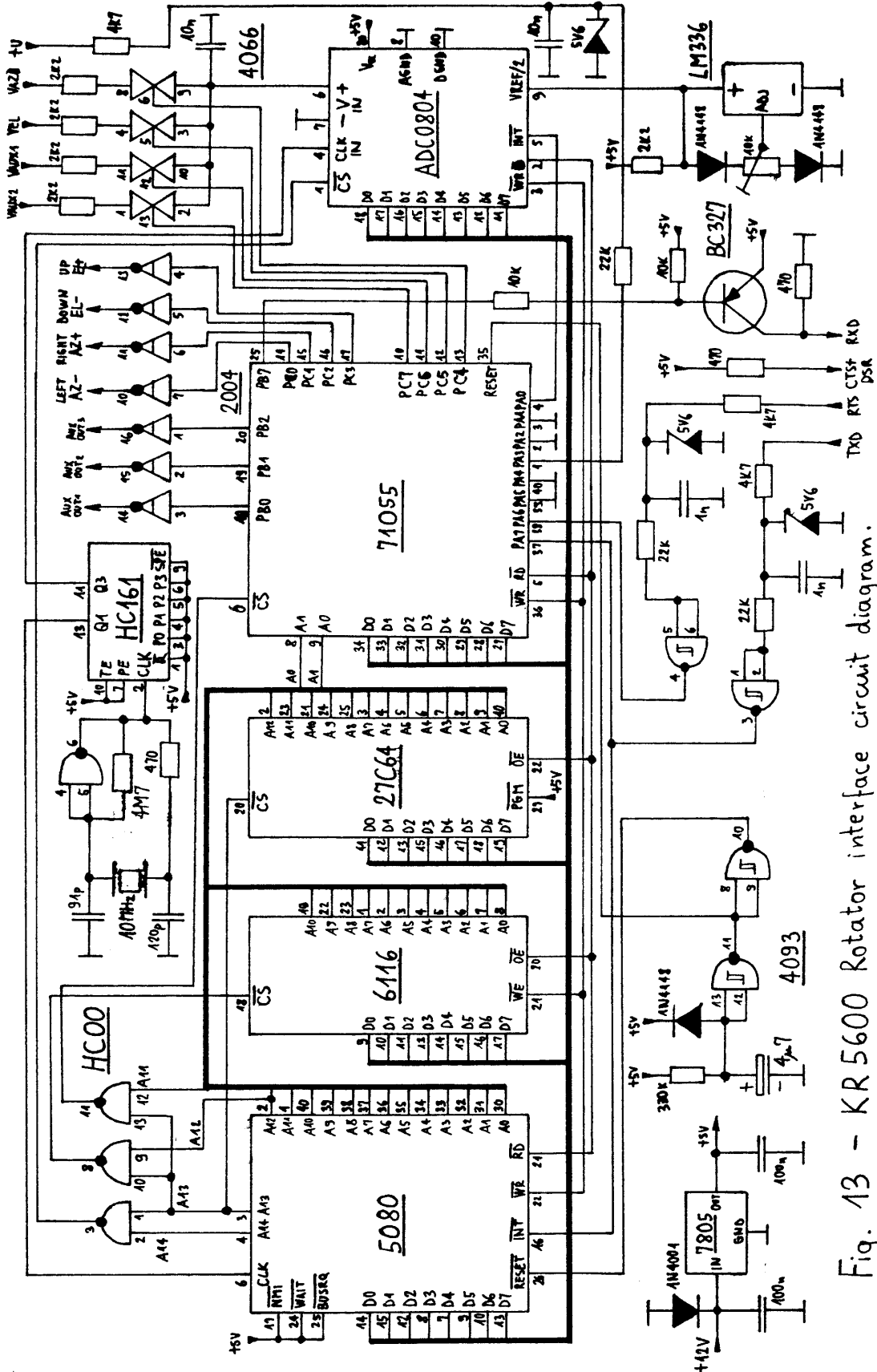
Fig. 12 – Power supply board circuit diagram.

Fig. 13 - KR 5600 Rotator interface circuit diagram.